

Fig. 1

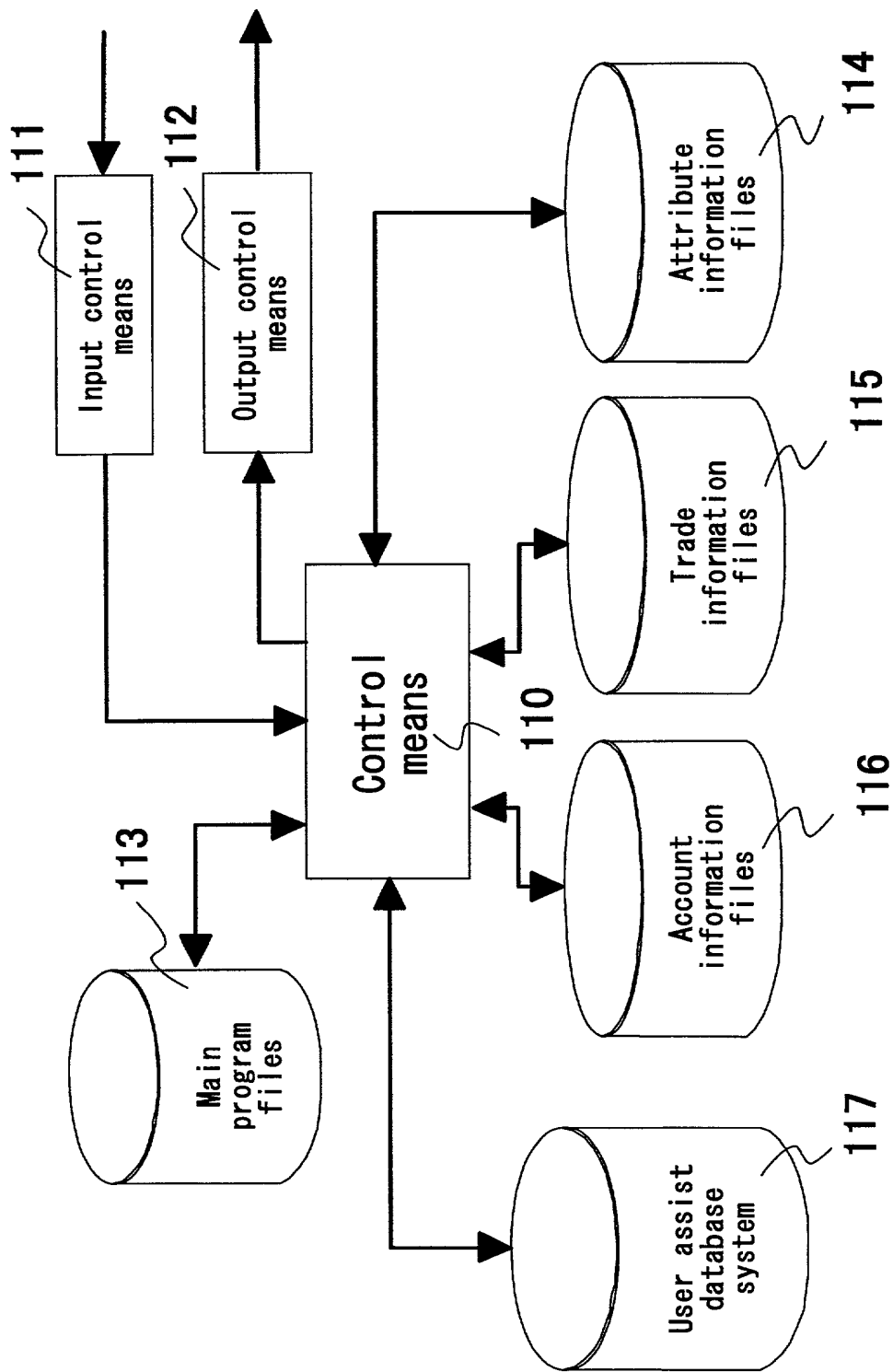


Fig. 2

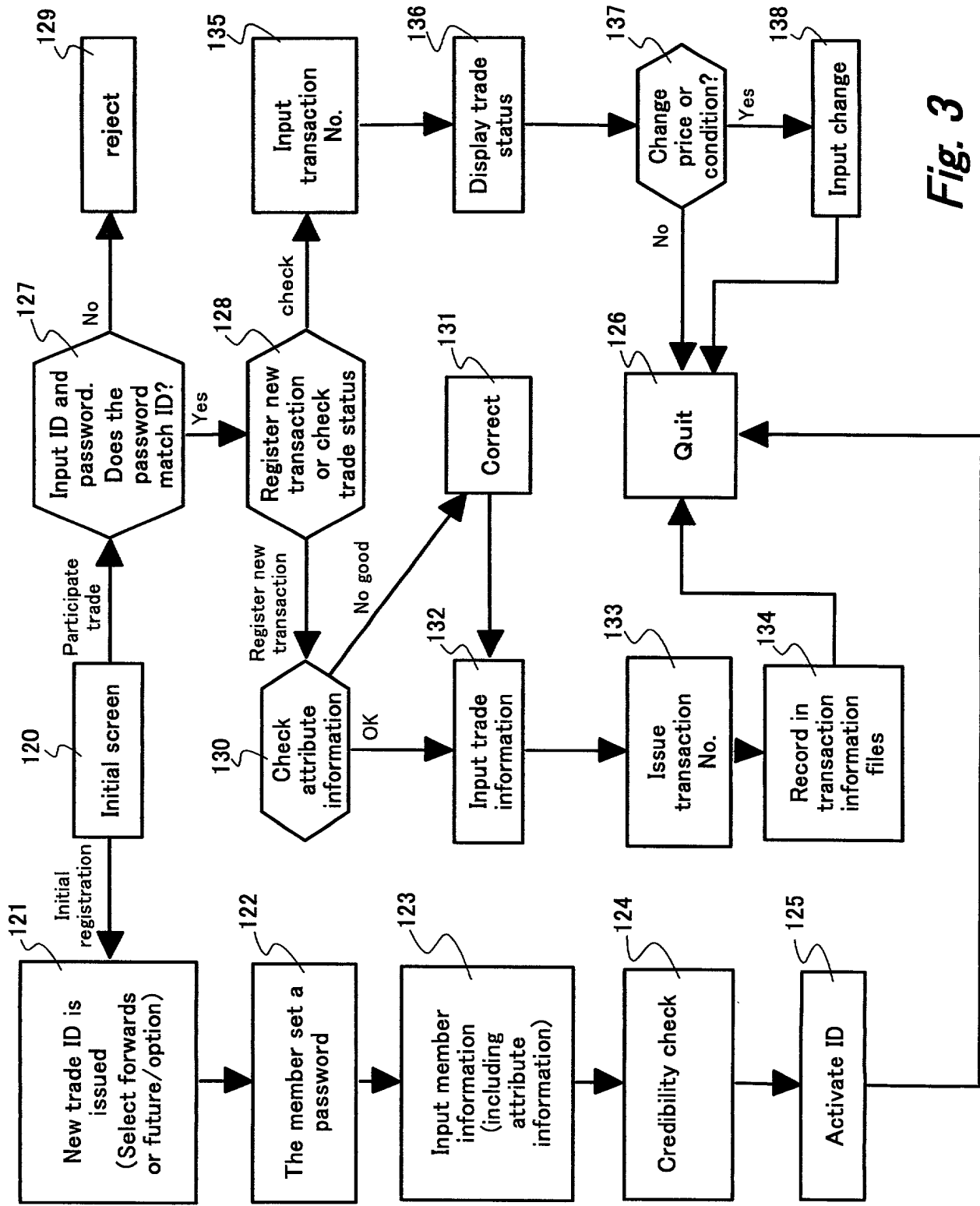


Fig. 3

member ID: 1003569 140

transaction ID: AZ4456321 141

company name: Japan LSI foundry Co. Fab 7 142

transaction type: selling capacity 145

specified price: 147

lowest price 1500 \$ 148

highest price none \$ 149

select highest offer 146

lot size: 2500 wafers 150

lot-in timing 2000/8/15 151

transaction dead line: 2000/8/1 152

information:

process type 0.18 micron CMOS

metal layer 6 layers

wafer size 8 inch

wafers per lot 23 wafers

max die size 1.45 X 1.45 mm

average TAT 4 weeks

show detail information 144

finish 153

Fig. 4

member ID:	1003569
company name:	Japan LSI foundry Co. Fab 7
manufacturing line information:	
wafer size	8 inch
wafers per lot	23 wafers
max die size	1.45 X 1.45 mm
average yield for TEG	87.6%
avarage TAT	4 weeks
max capacity	10000 wafers/month
process parameters:	
process type	0.18 micron CMOS
gate length	0.18 micron
gate type	polysilicon
metal pitch	2.0 micron
metal type	copper
metal layer	6 layers
min. pad pitch	30 micron
transistor threshold(P)	0.14 V
transistor threshold(N)	0.16 V
switching delay	400 p sec
max. clock rate	800MHz
suply voltage	1.25V
max gate size	5 million
	:
	:

Fig. 5

member ID: 1003569

company name: Japan LSI foundry Co. Fab 7

manufacturing line information

wafer size 8 inch

wafers per lot 23 wafers

max die size 1.45 X 1.45 mm

average yield for TEG 87.6 %

average TAT 4 weeks

max capacity 10000 wafers/month

process type 0.18 micron CMOS

gate length 0.18 micron

gate type polysilicon

metal pitch 2.0 micron

metal type copper

metal layer 6 layers

min. pad pitch 30 micron

transistor threshold(P) 0.14 V

transistor threshold(N) 0.16 V

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Fig. 6

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アドレス(A) http://silicontrade.com/registration/user.asist

検索(E) asahi(B) BCG Tokyo(E) Excite(E) infoseek(E) Yahoo!(E) jcom(E) palto-city(E)

member ID: 1013644

company name: Japan Compter Systems Co.

process type 0.18 micron CMOS

used library Artisan

I/O signals 265 pins

max. clock rate 800 MHz

suply voltage 1.8 V

gate size 1.2 million

digital IP ARM7TDMI, DRAM512k byte

analog IP oscillator, PLL, delta sigma A/D converters(30MSPS)

number of chips 500,000 units

dead line September 11, 2000

finish

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Fig. 7

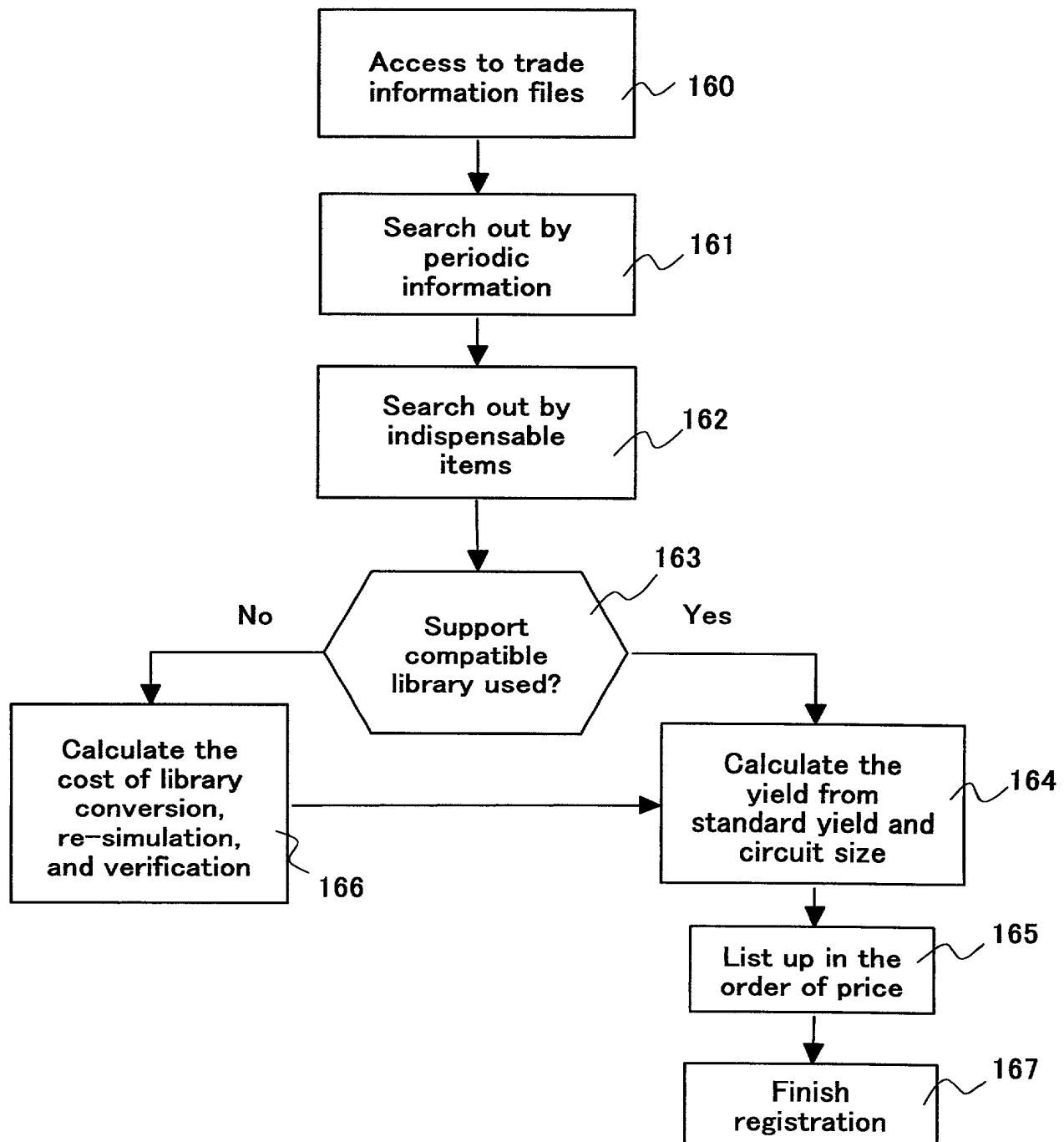


Fig. 8

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http://Silicontrade.com/registration/tech_service

member ID: 1020031

company name: Tokyo IP Design Co.

specialized area

telecommunication IPs

past design

Bluetooth base band

PDC baseband

cdmaOne baseband

Japan Design Qualification Service Co.

quality auditor

design quality

AA

AAA

B

support quality

B

AA

AAA

finish

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Fig. 9